IP TELEPHONE SYSTEM

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Application No. 09/986,752 filed on November 9, 2001, which claims the benefit of U.S. Provisional Application No. 60/246,991, filed on November 9, 2000, both of which are incorporated by reference herein in their entireties.

[0002] This application also claims benefit of U.S. Provisional Application No. 60/258,777, filed on December 28, 2000, which is incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0003] The present invention is related to a communications device. More specifically, the present invention is related to an IP telephone having an on-chip native device relay, and an on-chip filter termination for a constant impedance filter that is located off-chip.

Background Art

[0004] In addition to data communications, the Internet can also be used to carry voice telephony. One conventional system that carries voice communications over the Internet utilizes an Internet Protocol (IP), and such telephones are referred to as IP telephones.

[0005] The data terminal equipment (DTE) of an IP telephone includes a telephone line that is connected to a computer device through a series-connected

relay (i.e. switch). The relay switches an incoming telephone signal to either the computer or to a filter that is connected in parallel with the computer. The filter is connected/disconnected across the computer depending on the state of the IP phone system by closing/opening the associated relay. In a no power or "discovery" mode, the relay is switched so the filter is connected across a physical layer input of the computer. Therefore, the filter receives an incoming signal on the telephone line and reflects low frequency signals back down the telephone line, without the incoming signal reaching the physical layer of the computer. The reflected low frequency signals indicate that a compatible IP phone is available for use. When power is applied to the relay in a "normal operation" mode, the relay is switched so the filter is disconnected from the input of the physical layer of the computer. Therefore, the filter does not effect the incoming signal, and the incoming signal is applied to the physical layer of the computer for further processing.

[0006] The continual opening and closing of the relay creates wear and tear of the relay components as the conventional IP phone switches between the discovery and normal modes, eventually causing component failure. It would be more cost-effective to keep the filter connected at all times, thereby eliminating relay replacement. Additionally, the conventional relay is not integrated with the computer or the filter, which increases the manufacturing part count and ultimately the manufacturing cost of an IP Phone.

[0007] The conventional IP telephone also includes a signal termination circuit that provides a good input impedance for the incoming signal when the filter is not connected across the computer. Proper signal termination is necessary to provide a good signal match, which aids in proper signal reception during the normal operation mode. The termination circuit is a separate off-chip device, which increases the manufacturing part count and ultimately the manufacturing cost of an IP Phone. It is desirable to integrate the termination circuit in order to reduce the part count during the manufacturing process.

[0008] The filter in the conventional IP telephone is a conventional lowpass filter. The conventional lowpass filter has an input impedance that is highly dependent on the frequency of the input signal that is delivered to the filter. Input frequencies that are outside of the filter passband are substantially reflected, which can produce an undesired high return loss. Also, conventional filters are highly sensitive to variations in the filter components and in the variation of components that are connected to the filter.

[0009] What is needed is a filter that has a constant impedance for all frequencies, even frequencies that are outside the passband of the filter. Furthermore, the filter should be relatively insensitive to component variation.

BRIEF SUMMARY OF THE INVENTION

[0010] The present invention relates to a communication device that is capable of being connected to a communications network. The communications device can be, for example, an internet protocol (IP) telephone that is connected to an IP telephone network. The internet protocol telephone includes a substrate having an input and an output that are capable of being connected to the internet protocol (IP) network. A filter is external to the substrate, and is coupled to the input. A switchable termination is disposed on the substrate and across an output of the filter. The switchable termination provides a constant input impedance at an input of the filter when it is applied during the normal operation mode. A relay is disposed on the substrate and is connected between the input and the output of the substrate. The relay includes first and second native FETs that have a threshold voltage of approximately zero volts. Therefore, the relay is nominally turned-on, even when little or no voltage (or power) is applied to the IP telephone substrate, as during the discovery mode of IP telephone operation. Rectifier circuits rectify an input signal received at an input of the filter, to produce a rectified signal that is applied to the gates of the first and second native FETs, so as to further

improve the conductivity of the relay. Grounding circuits ground the respective gates of the native FETs when a supply voltage is applied to the substrate, as during normal operations mode of IP telephone system operation. Additional grounding circuits also ground the gates of the native FETs in the rectifier circuits when the supply voltage is applied to the substrate.

[0011] The filter in the present invention filters out unwanted frequency signals by passing only desired frequency signals through the filter, and terminating undesired signals. The filter can remain connected to the system during both the discovery mode and the normal operation mode, because it has a substantially constant input impedance. The filter is configured to maintain a constant impedance through the entire filter for substantially all input frequencies. The filter may have several embodiments depending on the type of frequency signals that are being processed. A single ended filter may be one of the embodiments, where a plurality of poles are connected in series. The poles comprise an inductor, a capacitor and a resistor connected to the ground. Another embodiment may be a differential filter, where another inductor connects the poles. Yet another embodiment may be a band pass filter having a low pass circuit with a high pass circuit connected to it. The filter minimizes a return loss problem that is common in the conventional filters.

[0012] External relays are eliminated by leaving the filter connected to the relay and to the substrate. This reduces manufacturing and maintenance costs that are associated with these external relays that are used in conventional IP telephone systems.

[0013] Furthermore, the relay, the termination, the rectifier circuits, and the gate grounding devices can be configured on a single integrated circuit substrate. For example, the substrate can be a standard CMOS substrate. The filter can be external to the substrate, but the filter termination is configured on the substrate. The substrate can be part of the physical layer of a computer chip in the IP

telephone. For example, the computer chip could process voice and data communications with an IP network that is connected to the IP telephone.

[0014] Further features and advantages of the invention, as well as structure and operation of various embodiments of the invention, are disclosed in detail below will reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0015] The present invention is described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

[0016] FIG. 1a illustrates a conventional IP telephone, wherein a filter is placed between two relays, and termination resistors are placed outside a computer chip.

[0017] FIG. 1b illustrates a block diagram of a conventional IP telephone in discovery mode.

[0018] FIG. 1c illustrates a conventional IP telephone in normal operation mode.

[0019] FIG. 2a illustrates an IP telephone having a filter connected to the computer, according to embodiments of the present invention.

[0020] FIG. 2b illustrates a block diagram of an IP telephone according to the present invention.

[0021] FIG. 2c is another embodiment of a present invention IP telephone system.

[0022] FIG. 2d illustrates a block diagram of an IP telephone in discovery mode, according to embodiments of the present invention.

[0023] FIG. 2e illustrates a block diagram of an IP telephone in normal operation mode, according to embodiments of the present invention.

[0024] FIG. 3a illustrates a conventional low pass RL filter.

[0025] FIG. 3b illustrates a conventional low pass RC filter.

[0026] FIG. 3c illustrates a low pass and a high pass filter.

[0027] FIG. 3d illustrates a conventional Butterworth filter.

[0028] FIG. 4a illustrates a block diagram of the filter functions in the present invention.

[0029] FIG. 4b illustrates a multi-pole constant impedance low pass filter, according to embodiments of the present invention.

[0030] FIG. 4c illustrates a multi-pole constant impedance bandpass filter, according to embodiments of the present invention.

[0031] FIG. 4d illustrates a multi-pole constant impedance differential low pass filter, according to embodiments of the present invention.

[0032] FIG. 4e illustrates a second multi-pole constant impedance differential low pass filter, according to embodiments of the present invention.

[0033] FIG. 5a further illustrates a present invention relay.

[0034] FIG. 5b illustrates another embodiment of the relay in the present invention.

[0035] FIG. 5c illustrates another embodiment of the relay in the present invention.

[0036] FIG. 5d illustrates another embodiment of the relay in the present invention.

[0037] FIG. 5e illustrates another embodiment of the relay in the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Conventional Internet Protocol Telephone

[0038] FIG. la illustrates a conventional IP telephone system 125 having a data network 110 and a conventional IP telephone 100. The data network 110 can be the publically available Internet, or another type of public or private network.

The IP telephone 100 receives signals 102 from the network 110 at an input terminal 105, and transmits signals 103 to the data network 110 at the output terminal 106. In embodiments, the signals 102 and 103 carry voice communications using Internet Protocol.

[0039] The IP telephone 100 includes a filter 104, relays 120 and 121, and a physical layer 101 that is part of a computer chip (not shown) or other type of integrated circuit. The computer chip processes voice and data signals that are sent to and received from the data network 110. The relay 120 connects the input terminal 105 to either the filter 104 or an input terminal 108 of the physical layer 101. Likewise, the relay 121 connects the output terminal 106 to either the filter 104 or an output 109 of the physical layer 101. The relays 120 and 121 are nominally connected to the filter 104 when no power is applied to the relays. (i.e., discovery mode) When power is applied, the relays 120 and 121 switch and connect the terminals 105 and 106 to the respective terminals 108 and 109 of the physical layer 101 (i.e., normal operation mode). Grounded termination resistors 122 and 123 are inserted between the filter 104 and physical layer 101 to provide a good match and prevent unwanted signal reflections from affecting the input and output signals 102 and 103.

[0040] FIG. 1b further describes the operation of the IP phone in discovery mode, where no power is applied to either the relays 120, 121, or the physical layer 101. During discovery mode (FIG. 1b), the relay 120 connects the input terminal 105 to the input of the filter 104, and the relay 121 connects the output of the filter 104 to the output terminal 106. Therefore, the input signal 102 is filtered by the filter 104 and the filtered output is re-transmitted to data network 110 as the transmit signal 103. The filter 104 is configured as a lowpass filter with a pre-determined cutoff frequency that is compatible with the data network 110. In discovery mode, the data network 110 analyzes the transmit signal 103 for the correct low frequency components to determine that the IP phone 100 is compatible for future communication.

[0041] FIG. 1c further describes the operation of the IP phone 100 in normal operation mode, where power is applied to the relays 120, 121, and the physical layer 101. During normal operation (FIG. 1c), the relay 120 switches the input terminal 105 from the filter 104 to the physical layer input 108. Likewise, the relay 121 switches the output terminal 106 from the filter 104 to the output 109 of the physical layer 101. Therefore the physical layer input 108 is connected to the receive terminal 105, and the physical layer output 109 is connected to the output terminal 106 so that communication with the network 110 can commence. The resistor 122 should be highly accurate as the impedance of this resistor circuit must be matched with the impedance of the physical layer to prevent signal mismatch.

[0042] The IP phone 100 is relatively expensive to implement because the relay mechanisms 120 and 121, and the termination resistors 122 and 123 are located outside the physical layer 101, resulting in increased assembly cost.

IP Phone system with On-Chip Relay and Constant Impedance Filter

[0043] FIG. 2a illustrates IP telephone 200 according to embodiments of the present invention. IP telephone 200 has on-chip relays and a constant impedance filter according to embodiments of the present invention. The IP telephone 200 receives signals 201 from the network 110 at an input terminal 202, and transmits signals 214 to the network 110 at an output terminal 213.

[0044] IP telephone 200 includes a first termination resistor 212, a filter 204, and a physical layer 208 that is part of a computer chip (not shown), or other IC. The physical layer 208 can be implemented on a semiconductor substrate, for example and CMOS substrate. The physical layer 208 includes a second termination resistor 206, a switch 205, and a relay 210 that are all located on the physical layer 208, which is distinct from the conventional IP phone 100 that has the relays and both termination resistors located off-chip. Furthermore, the filter 204

is permanently connected to an input terminal 202 of the IP phone 200. Therefore, the filter 204 is not switched in and out of the receive path, as in the conventional IP phone 100. The filter 204 could be another type of circuit external to the physical layer 208.

[0045] The relay 210 includes a native MOSFET device, which has a threshold voltage that is equal to substantially zero volts. Therefore, the relay 210 conducts even when no voltage is applied to the gate of relay 210. Whereas, the switch 205 is conventional MOSFET device that requires a non-zero voltage source to close the switch 205. The properties of the relay 210 and native devices are further described herein.

[0046] FIG. 2d further describes the operation of the IP phone 200 in discovery mode, where no power is applied to the physical layer 208.

[0047] During discovery mode, the filter 204 receives the input signal 201 and generates a filtered output signal 215 that is applied to the physical layer 208 at terminal 209. The relay 210 is closed during discovery mode so that the filtered output signal 215 is transmitted to the data network 110 as the output signal 214. The filter 204 is configured as a lowpass filter with a pre-determined cutoff frequency that is compatible with the data network 110. In discovery mode, the data network 110 analyzes the transmit signal 214 for the correct low frequency components to determine that the IP phone 200 is compatible for future communication. The input signal 201 is also received at the physical layer input terminal 203. However, no power is applied to the physical layer 208 during discovery mode, so the A/D 250 and receiver 251 are not powered up. Therefore, the input signal 201 is not further processed by the physical layer 208 during discovery mode.

[0048] FIG. 2e further describes the operation of the IP phone 200 in normal operation mode, where power is applied to the physical layer 208. During normal operation, power is applied to the physical layer 208, which opens the relay 210 and closes the switch 205. By opening the relay 210, the filter output 215 is not

re-transmitted to the data network 110. However, the physical layer 208 is powered-up so that the input signal 201 is received at the physical layer 208. There is no need for an extra termination resistor located off-chip, such as termination resistor 122 of FIG. 1c, because the impedance of the filter 204 and the termination resistor 206 matches the input impedance. As will be described later with respect to the filter 204, the filter 204 is insensitive to component variation. Therefore, the termination resistor 206 can be placed on-chip and does not affect filter 204 frequency response or impedance of the filter 204. The filter 204 and the termination resistor 206 serve to properly terminate the signal on-chip. Furthermore, the analog-to-digital converter 250 and the receiver 251 further process the signal 201. More specifically, the analog to digital converter 250 samples and encodes the analog signal to create a digital signal. The process may be accomplished by a digital signal processor (DSP). The receiver 251 is a device that receives a transmission signal. The receiver 251 may also be described as a portion of a telecommunications devices that decodes an encoded signal into a desired for. For example, the receiver 251 process the digital signal from the analog to digital converter 250 to extract useful information from the data network 110. Furthermore, the physical layer output terminal 211 is still directly connected to the output terminal 213. Therefore, normal communications are carried-on with the network 110 through the input terminal 202 and output terminal 213.

[0049] A high-level diagram of the constant impedance filter 204 is shown in FIG. 4a. The filter 204 accepts the input signal 201 and selects a band of frequencies in the filter output 215 that are passed to the input 209 of the physical layer 208. Furthermore, the filter 204 terminates any undesired frequencies 492 that are not passed to the output 212. The filter 204 is described further in following sections.

[0050] Other embodiments of the Internet Protocol system are possible, however, the above is a description of one embodiment and not to be construed as limiting the scope of the present invention, except as designated by the claims that follow.

Relay

[0051] FIG. 2b further illustrates the physical layer 208 that has the relay 210 and the termination resistor 206. The physical layer 208 is illustrated in a differential implementation, as compared to a single-ended implementation. The termination resistor 206 is connected to the output of the filter 204 via input terminals 233, 234, where terminals 233, 234 represent a differential input for input 216. The termination resistor 206 is implemented with resistors 271, 272, and PMOSFET 273. The relay 210 is connected to the output of the termination resistor 206, and is implemented with output native devices 235 and 236. The output native devices 235 and 236 are connected to respective output terminals 237 and 238, where terminals 237 and 238 represent a differential output for output 211 in FIG. 2b.

[0052] Furthermore, the physical layer 208 also includes rectifier circuits 225 and 226, and PMOSFETs 231 and 232. The rectifier circuit 225 includes a resistor 227 and a native device 228. The input of the rectifier circuit 225 is connected to the input terminal 221 via filter pin 223, and output is connected to the gate of the output native device 235 through PMOSFET 231. Likewise, the input of the rectifier circuit 226 is connected to the input terminal 222 via filter pin 224, and the output is connected to the gate of the output native device 236 through PFET 232. As will be discussed further herein, the rectifier circuits 225 and 226 rectify the input 201 and apply the rectified signal to the gate terminals of the native devices 235, and 236, so as to further turn-on the relay 210 during the discovery mode. PFETs 231 and 232 are biased to conduct during the discovery mode, so as to apply the rectified outputs from the rectifiers 225 and 226 to the gates of the

respective output native devices 235 and 236. However, the PFETs 231 and 232 are biased to be cutoff during normal operation mode, so as to prevent the rectified outputs from the rectifiers 225 and 226 from reaching the gates of the respective output native devices 235 and 236. Additionally, the output native devices 235 and 236 are biased such that in normal operation mode, the gate-to-source voltage, V_{gs}, is a negative voltage. This ensures that the native devices are turned off. This is done by grounding the gate of the native devices and holding drain and source at the supply voltage.

[0053] In the discovery mode, when no power is applied to the physical layer 208, the relay 210 passes through signals 201 to allow for signal detection by the network 110. However, in the normal operation mode, when the physical layer 208 is powered up, the relay 210 does not allow passage of signals through to the network 110. Furthermore, the relay 210 serves to prevent any possible "leakage" of signals through the relay and minimize the return loss during the normal operation mode. The relay 210 is constructed using native devices, which are capable of operating without any power applied to them. This allows for better conductivity of the relay and faster detection of the signal by the network 110 during the discovery mode. In the normal operation mode, the native devices are grounded using additional semiconductor devices. These additional devices operate with application of voltage to them, while the sources and drains of the native devices are held at the supply voltage. The details of the relay schematic and its implementation in the discovery and the normal operation modes are discussed below.

Discovery Mode

[0054] In the discovery mode, (as described by FIG. 2d), the physical layer 208 functions without any power applied to it. The relay 210 is closed in order to facilitate detection of a filtered signal 215 by the network 110. More specifically,

the output native device 235 and 236 are closed. The differential signal received at the input terminals 221 and 222 (similar to receive input 202 of FIG. 2a) is filtered through the constant impedance filter 204 and passed through the relay 210. The output of the relay 210 is transmitted out through transmit output terminals 237 and 238 (similar to the output terminal 213 of FIG. 2a) and is detected by the network 110. In the discovery mode, the relay 210 is capable of rectifying the filtered signal 215 thereby increasing a voltage on the native devices, which it employs, and increasing general conductivity of the relay 210.

[0055] As previously mentioned, the relay 210 uses native devices. The native device, NMOSFET or NMOS (n-channel metal oxide semiconductor field effect transistor), is a device that has a quality of being conductive when no bias voltage is applied. In other words, the threshold voltage, V_{thresh}, is equal to zero. In one embodiment, the threshold voltage of the native device is approximately from −100mV to +100 mV. Whereas, conventional relays employ regular MOSFET devices. Conventional MOSFET devices require a bias voltage to put them in the conductive state, i.e., a standard depletion voltage of about 400mV is needed. The use of native devices creates a better relay that is capable of being closed during the discovery mode. In other words, no voltage is required to close the relay, and the relay is open during the normal operation mode by application of a voltage to the physical layer.

[0056] The physical layer 208 includes rectifier circuits that rectify the input signal 207, and apply the rectified voltage to the gate of the output native devices 235 and 236. Referring to FIG. 2b, two rectifier circuits 225 and 226 are shown connected to the filter pins 223 and 224, respectively. The filtered signal 215 is passed through the rectifier circuits 225 and 226, where it is rectified. The rectifier circuit 225 consists of a native device 228 and a resistor 227. The rectifier circuit 226 consists of a native device 230 and a resistor 229. The rectifier circuits 225 and 226 are connected to a pair of output native devices 235 and 236, respectively, as shown in FIG. 2b.

[0057] PFET 231, connected between the rectifier circuit 225 and the output native device 235 is not engaged in the discovery mode, thereby allowing direct connection between the rectifier circuit 225 and the output native device 235. PFET 232, connected between the rectifier circuit 226 and the output native device 236 is not engaged in the discovery mode, thereby allowing direct connection between the rectifier circuit 226 and the output native device 236. Since, the rectifier circuits 225 and 226 are using native devices to rectify the filtered signal 215, such rectification increases amplitude of the signal 201, which increases the voltage on the gates of the output native devices 235 and 236. This increases the general conductivity of the relay and faster detection of signal by the output terminals 237 and 238. This provides for faster detection of the signal at the output terminals 237 and 238 and, hence, the network 110. Such detection of the signal by the network 110 alerts the network of the presence of the compatible IP telephone system 200, placing the entire system into the normal operation mode.

[0058] The relay 210 is shown in more detail in FIG. 5a. The embodiment shown in FIG. 5a is one of the four embodiments that the relay 210 may take (others are shown in FIGS. 5b-5e and will be described later). FIG. 5a, as well as FIGS. 5b-5e, show a portion 590 of the physical layer 208. In this embodiment, the relay 210 has positive and negative input terminals 233 and 234 as well as positive and negative output terminals 237 and 238, respectively (as also shown in FIG. 2b). The positive terminal 233 is connected to the rectifier circuit 225 and the negative terminal 234 is connected to the rectifier circuit 226. Each of the rectifier circuits are described above in reference to FIG. 2b. The rectifier circuits 225 and 226 are connected to the output native devices 235 and 236 having a common gate connection 510. As stated above, the PMOS devices 231 and 232, which are active in the normal operation mode, are not engaged in the discovery mode. These devices 231 and 232 serve to ground the gates of native devices 230 and 228 during the normal operation mode. Furthermore, another series of gate

grounding devices 262, 263 and 264 are added. These devices are conventionally known NMOS devices and are also employed during the normal operation mode. These devices serve to ground the common gate connection 510.

[0059] Referring to FIG. 5a, the filtered signal 215 is received at the input terminals 233 and 234. The rectifier circuits 225 and 226 rectify the signal 215 and increase its amplitude. The PFETs 231 and 232 are biased closed during discovery mode. Therefore, the output of 226 and 227 are applied to 510, which increases the voltage at the common gate connection 510. This, in turn, increases gate voltage on the output native devices 235 and 236 making these native devices more conductive, which increases conductivity of the entire relay 210.

[0060] The embodiment depicted in FIG. 5a does not account for a possible delay in transmission of a signal from the filter during the discovery mode. Referring to FIG. 5b, another embodiment of the relay is shown. This embodiment of the relay 210 accounts for a possible delay of signal transmission within the filter. Here, the relay 210 is shown to have input terminals 530 directly connected to output native devices 535 (similar to output native devices 235 and 236 of FIG. 2b) and output terminal pads 540. The relay 210 rectifier circuits 520 (similar to rectifier circuits 225 and 226 in FIG. 2b) are directly attached to the filter pins 541, which in turn are connected to the constant impedance filter 204 (not shown). Each rectifier circuit 520 comprises a resistor 521 and a native device 522, as shown in FIG. 5b. The rectifier circuits 520 are further connected to PMOS devices 524, which serve to ground the gates of native devices 522 during the normal operation mode (similar to devices 231 and 232 in FIG. 2b). These devices (as well as gate grounding devices 536 with respect to the gates of the native devices 535) do not ground the gates of native devices 522 during the discovery mode, since no power is applied to turn the devices 524 on. The devices 524 and 536 and their functions will be described later in connection to the normal operation mode.

[0061] With respect to FIG. 5b, an incoming signal would come directly to the rectifier device 522 and PMOS device 524, bypassing the filter off-chip. This reduces or eliminates any signal delay caused by the rectifiers. By the time the signal passes through the filter 204 and comes through the input 530 and reaches the output native devices 535, the rectifier 522 and PMOS device 524 have already conditioned the signal and have turned on the native devices 535 by applying the rectified signal at the gate of the native device 535. Subsequently, the voltage on the gates of the native devices 535 is increased, making these devices more conductive, thus, increasing conductivity of the entire relay 210.

[0062] FIG. 5e illustrates another embodiment of the relay portion 590, where PFET 231 and PFET 232 are cross-connected. More specifically, the gate of the PFET 231 is connected to the drain of the PFET 232 at node 572. Furthermore, the gate of the PFET 232 is connected to the drain of the PFET 231 at a node 571. This connection improves the operation of the rectifier circuits 226 and 225 during discovery mode. Since the input signal 215 is differential, one of the terminals 233 and 234 receives a positive voltage and the other terminal receives a negative voltage at any give time. By cross-connecting the PFETs 231 and 232, the V_{GS} of at least one these PFETs will be positive at any given time, regardless of the current polarity of the input signal 215. Therefore, the PFETs 231 and 232 will turn on faster and stronger during the discovery mode than without the cross-connection.

Normal Operation Mode

[0063] After the signal is detected by the network 110 in the discovery mode, the IP telephone system 200 is placed in the normal operation mode, where a voltage source (typically on the order of 3V) is applied to the physical layer 208, including the input terminals 233, 234 and output terminals 237, 238. In the normal operation mode, the physical layer 208 is powered up, thereby opening

the relay 210 and closing switch 205. Since, the filter 204 remains connected to the IP telephone system 200 during the normal operation mode, it is desirable to prevent any leakage of signals through the relay 210 to the transmit output 211 (FIGS. 2a and 2e). Therefore, the relay 210 is constructed as to not allow any signals pass through it to the network 110 during the normal operation mode (FIG. 2a).

[0064] In the normal operation mode (as described by FIG. 2e), an incoming signal 201 is terminated in a termination resistor 206 after being passed through the constant impedance filter 204, as shown in FIG. 2b. In the normal operation mode, the native devices 228 and 230 and output native devices 235 and 236 are grounded. Therefore, no signal passes through to the output terminals 237 and 238. The PMOS devices 231 and 232, which are turned off by application of voltage, cutoff the rectifier outputs of the rectifier circuits 225 and 226. The PMOS devices 231 and 232 serve to minimize a "leakage" of rectified signals through to the output native devices 235 and 236 during the normal operation mode. Because the gates of output native devices 235 and 236 are grounded and the sources and drains are held at supply voltage, no signal is able to pass through the relay 210, thereby opening relay 210 during the normal operation mode. Moreover, the series of gate grounding devices 262, 263, and 264 ground the gates of the output native devices 235 and 236.

[0065] Referring to FIGS. 2b and 5a, the gate grounding devices 262-264 are attached to power sources (an analog digital voltage source 261 and an analog digital ground 207) of the physical layer 208. Referring to FIG. 5a, during the normal operation mode, a voltage source is applied to terminals 261 to turn the gate grounding devices 262-264 on. This, in turn, grounds the gate connection 510 by shorting gate 510 to ground 207, thereby grounding the gates of the output native devices 235 and 236. Native devices 235 and 236 are cutoff by grounding of their respective gates. The gate grounding devices 262-264 are typically

NMOS devices, however, other semiconductor devices may be substituted instead, depending on the particular requirements of a circuit.

[0066] Furthermore, referring to FIG. 5a, the PMOS devices 231 and 232 (which are attached to the native devices 228 and 230 in the rectifier circuits 225 and 226, respectively) are attached to the analog digital voltage source 261 of the physical layer 208. Therefore, in the normal operation mode, the devices 231 and 232 are raised to the level of potential applied to the physical layer 208, thus, cutting off the rectifier circuits 225 and 226 from the output native devices 235 and 236.

[0067] Since, the gates of native devices 228 and 230 and the output native devices 235 and 236 are grounded, and their respective sources and drains are held at supply voltage, no signal is capable of passing through the relay 210 (as was also described in reference to FIG. 2b). Any signal that passes through the constant impedance filter 204 is terminated in the termination resistor 206, as shown in FIG. 2b. In the IP phone 200, the only termination resistor outside the physical layer 208 is a resistor 212 connected between the transmitting output 213 and the physical layer output terminal 211. There is no termination resistor that is connected between the input terminal 202 and the receiving input 203. Therefore, the amplitude of the signal 201 is not reduced during discovery mode since the signal is not terminated prior to the filter 204. Furthermore, the on-chip termination 206 only becomes effective after power is applied during the normal operation mode. This can be referred to as a dynamic termination, since the on chip termination occurs only when the power is applied and the switch 205 is closed. Referring to FIG. 2b, the on-chip termination resistor 206 is shown in more detail. The structure consists of a pair of resistors 271 and 272 and a PMOS device 273 connected to an analog digital ground 207 of the physical layer 208.

[0068] With respect to the embodiment depicted in FIG. 5b, the relay 210 operates similarly in the normal operation mode as its embodiment described in FIG. 5a. The relay 210 has PMOS devices 524 (similar to devices 231 and 232

of FIG. 2b) connected to the analog digital voltage source 261 of the physical layer 208. The PMOS devices 524 ground the gates of the native devices 522 during the normal operation mode. Furthermore, to ensure non-conductivity of the relay the gate grounding devices 536 (which are connected to the digital analog voltage source 261 and the digital analog ground 207) ground a gate connection 539, thereby grounding output native devices 535 (similar to the gate grounding devices 262-264 with respect to the output native devices 235 and 236 in FIG. 2b).

[0069] The embodiments of the relay 210 shown in FIGS. 5c and 5d are similar in circuit architecture to the embodiments shown in FIGS. 5a and 5b, respectively. These embodiments should be considered together with respect to FIG. 2c (similar to the schematic shown in FIG. 2b). In case of the embodiment shown in FIG. 5c, the relay's PMOS devices 231 and 232 have additional connections 281 and 282, where connection 281 is a connection between the source of the native device 228 and the PMOS device 231 (similarly connection 282 is a connection of the source of 230 and the PMOS device 232). This embodiment, as well as embodiment shown in FIG. 5d, allows for lower return loss of the relay 210 during the normal operation mode. Similar source connections are made, as is shown in FIG. 5d, where the source of the native device 522 is connected to the PMOS 524 at connection 551.

[0070] There are other embodiments of the relay are possible, however, these are some of the embodiments and not to be construed as limiting the scope of the invention, except by the following claims.

Constant Impedance Filter

[0071] Filters are commonly used to prevent unwanted frequencies from passing to communication devices. For example, a conventionally known low pass filter consists of an inductor connected in series with a resistor. Referring to FIG. 3a,

a low pass filter 301 (an *RL* filter) is shown to have an inductor 302 connected to a resistor 303, which is grounded. One problem with the lowpass filter 301 is that the input impedance of the filter 301 is a function of frequency, as illustrated by the equations (1) and (2) below:

$$Z = R + sL \tag{1}$$

$$|Z| = \sqrt{R^2 + (\omega L)^2} \tag{2}$$

wherein Z is the input impedance of the filter; R is resistance of the resistor 303; ω is angular frequency; and ωL is inductive reactance of the inductor 302. As shown by equations (1) and (2), the input impedance of the lowpass filter 301 varies with frequency. The variable input impedance causes a variable return loss, which can decrease signal performance if there is a need for constant impedance circuitry.

[0072] As illustrated in FIG. 3b, another low pass filter 310 is shown to have a resistor 311 connected to a capacitor 312 (a single pole). Low pass filter 310 also has impedance that varies with frequency as presented by equations (3) and (4):

$$Z = R + \frac{1}{sC} \tag{3}$$

$$|Z| = \sqrt{R^2 + (\frac{1}{\omega C})^2} \tag{4}$$

wherein C is the capacitance, R is resistance, ω is angular frequency, and $\frac{1}{\omega C}$ is capacitive reactance. As with the *RL filter*, the impedance of filter 310 varies with frequency, producing a variable return loss with frequency.

[0073] FIG. 3c illustrates a low pass and a high pass filter 320 that has a constant impedance at all frequencies. Filter 320 includes an inductor 321 that series

connected with a resistor 322. Inductor 321 and resistor 322 are further connected in parallel to a capacitor 323 that is series connected with resistor 326. This filter 320 is capable of maintaining the following relationship for substantially all frequencies:

$$Z = R \tag{5}$$

wherein Z is the input impedance and is a pure resistance R. In embodiments, R is the resistance of the resistors 322 and 326, or a parallel combination thereof. The impedance in equation (5) is derived from equations (6) and (7) that are recited below:

$$Z = \left\{ (R + sL)^{-1} + (R + \frac{1}{sC})^{-1} \right\}^{-1} \tag{6}$$

$$C = \frac{L}{R^2} \tag{7}$$

[0074] The filter 320 is only a one pole solution. A single pole may not provide enough attenuation and therefore may allow some unwanted frequencies to pass through the filter.

[0075] FIG. 3d illustrates a lowpass Butterworth filter 330. The filter 330 is a passive *LC* filter comprising of multiple poles (*LC* circuit groups). In one example, the Butterworth filter 330 is a 5-pole filter, wherein a pole includes an inductor 335 and a capacitor 336. The filter attenuation outside the passband of the filter 330 increases with the number of poles in the filter 330. However, as the number of poles in the Butterworth filter 330 increases, the filter response becomes more sensitive to component variations.

[0076] The impedance of the Butterworth filter 330 varies with frequency. Within the filter passband, the impedance of the filter is matched and the signals pass through. However, outside the passband, the impedance is high and the filter

becomes totally reflective. A Butterworth filter can be configured in a low pass, high pass, and a band pass variety.

[0077] FIGS. 4a-4e describe a constant impedance filter having multiple poles according to the present invention. A constant impedance filter maintains a constant input impedance through the filter for frequencies that are both inside and outside the filter passband. In other words, frequencies inside and outside the filter passband see a substantially matched impedance. Frequencies that are inside the filter passband are passed to the filter output. Frequencies that are outside the filter passband are terminated inside the filter, and are not reflected.

[0078] FIG. 4a illustrates the function of a filter 204 according to the present invention. The filter 204 receives an input signal 202 having multiple frequency components. The filter 204 terminates unwanted frequencies 492 from the input signal 202 into a matched impedance 412, and passes the desired frequencies 211 to the filter output 212. The input impedance for the filter 204 is constant for substantially all frequencies, including those frequencies that are outside the filter passband. In other words, the input impedance of the filter 204 appears to be completely resistive.

[0079] FIG. 4b illustrates a constant impedance lowpass filter 204 according to embodiments of the present invention. The filter 204 includes a plurality *RLC* circuit units or poles 410a, 410b, 410c, etc., that are connected in series with each other. Each *RLC* circuit unit 410 includes an inductor 405, a capacitor 406, and a resistor 407 and a ground 408, along with a plurality of other poles 410 ending with the termination resistor 206 and the PMOS relay device 273 (as described in FIG. 2b). For instance, a pole 410a will include an inductor 405a, a capacitor 406a, a resistor 407a, a ground 408a, and the plurality of poles 410 (such as 410b, 410c, etc.) along with the termination resistor 206 and the PMOS device 273. The input signals come through the input terminals 401 and are filtered through the chain of the *RLC* circuits 410, to an output 402. The termination resistor 206 is

connected between the PMOS relay device 273 (which is connected to the output 402) and the ground 207.

[0080] The filter poles 410 in the filter 204 provide a constant input impedance regardless of frequency, if equations (5)-(7) is satisfied. More specifically, the input impedance of each pole 410 is equal to the resistance of the respective resistor 407, as long as the capacitance 406 and inductor 405 are chosen according to the relationship in Equation 7. As a result, the filter 204 appears as a pure resistor to the incoming signal. Frequencies that are outside the passband of the filter 204 are terminated in a matched impedance, and are not reflected. Frequencies that are inside the passband of the filter 204 are passed to the output 402.

[0081] The angular frequency cutoff of each pole may be determined by the following relationship:

$$\omega = R / L \tag{8}$$

where, $\omega = 2\pi f$.

[0082] Each pole 410 can have the same frequency cutoff or each pole 410 can have a different cutoff frequency, depending on the specification of devices connected to the filter. If different cutoff frequencies are selected, then the effect of each pole 410 is cascaded over another pole 410. Nonetheless, the filter 204 would appear as a constant impedance filter across all frequencies as long the equations (5)-(7) are satisfied.

[0083] For a desired cutoff frequency and input impedance (which determines R), the values for L and C for each pole 410 can be calculated by solving equations 7 and 8. For example, if the desired input impedance is 100 ohm and the desired cutoff frequency is 2.274 MHz for a pole 410, then L is found using equation 8 and C is found using equation 7, where L is 7.0uH and C is 700pF.

[0084] As stated above, the cutoff frequencies of each pole 410 can be selected to be same, or the cutoff frequencies can be different in for each pole 410 in the

filter 204. Additionally, the resistors 407 can be identical for each pole 410 in the filter 204, or the resistors 407 can vary from one pole 410 to another pole 410. If the resistors vary from pole to pole, then input impedance at 401 is the based combination of the resistors 407 in each pole 410 and the termination resistor 206, assuming that equations (5)-(7) are satisfied in each pole.

[0085] In one embodiment, the resistor 407 is the same for each pole 410 and is equal to the termination resistor 206. In this embodiment, the input impedance at the terminal 401 is the resistance of the resistor 407, assuming equations (5)-(7) are satisfied.

[0086] Referring to FIG. 2b, the termination resistor 206 is configured using resistors 271 and 272 and a PMOS relay device 273 that is connected to ground terminal 207. The resistors 271 and 272 are connected across the terminals 233 and 234 when the PMOS relay 273 is closed. The resistors 271 and 272 provide a termination for the filter 204 when applied across the terminals 233 and 234. During discovery mode, no voltage is applied to the physical layer 208, so the terminal 207 is allowed to float open and the resistors 271 and 272 are not applied across the terminals 233 and 234. Therefore, the filter 204 is not terminated during the discovery mode, as represented by the open relay 205 in FIG.2d. In the normal operation mode, a ground voltage is applied at terminal 207 to the gate of the PMOS device 273, causing the PMOS device to conduct and apply the resistors 271 and 273 across the terminals 233 and 234. Therefore, the filter 204 is properly terminated during the normal operation mode, produce the desired constant impedance across all frequencies. Furthermore, in the normal operation mode, any signal that comes through the filter is terminated in the resistors 271 and 272 since the PMOS device 273 is closed and the relay 210 is open. The signal is analogously terminated in the following embodiments of the filter 204.

[0087] FIG. 4c illustrates a bandpass filter 204 that has a constant input impedance. Referring to FIG. 4c, the input signals come in through an input terminal 401 encountering a series of *RLC* circuit units or poles 420 (a, b, c, etc.).

Each pole 420 includes an inductor 423, a capacitor 424, and a resistor 425 and a ground 426, along with a plurality of other poles 420 ending with a termination resistor 206. For instance, a pole 420a will include an inductor 423a, a capacitor 424a, a resistor 425a, a ground 426a, along with a plurality of poles 420 (such as 420b, 420c, etc.) that end with the termination resistor 206 and the PMOS relay device 273. The chain of *RLC* poles 420 ends with the termination resistor 206, the PMOS relay device 273 and the ground 207. In the pole 420c, the resistor (not shown) is removed leaving only the capacitor 424c (as shown). A chain of highpass circuits or poles 430 (a, b, c, etc.) are attached to one terminal of the capacitor 424c, so as to be in parallel with the lowpass poles 420. Therefore, the lowpass poles 420a, 420b, and 420c includes a plurality of lowpass poles 420 and the plurality of highpass poles 430 along with respective termination resistors 206 and the PMOS relay devices 273. Subsequent lowpass poles 420 (i.e., 420d, 420e, etc.) include only the plurality of lowpass poles 420 and not the plurality of highpass poles 430. It is clear, that the plurality of highpass poles may be attached to the plurality of lowpass poles at any given lowpass pole 420. Each highpass pole 430 includes an inductor 432, a capacitor 431, and a resistor 433 and a ground 434 along with a plurality of other poles 430 ending with the termination resistor 206 and the PMOS relay device 273. For instance, a pole 430a will include an inductor 432a, a capacitor 431a, a resistor 433a, a ground 434a, and the plurality of poles 430 (such as 430b, 430c, etc.) along with the termination resistor 206 and the PMOS device 273. The filter 204, shown in FIG. 4c, has a bandpass response determined by the lowpass cutoff frequency of the poles 420, and by the highpass cutoff frequency of the poles 430. The cutoff frequency of the lowpass poles 420 and the highpass poles 430 are determined by the equation 8. As in FIG. 4b, the inductor and capacitors in the lowpass poles 420 and the highpass poles 430 can be selected to provide a constant input impedance for each pole 420, 430 by satisfying Equation (5)-(7). If the lowpass poles 420 and the highpass poles 430 are selected to have the same constant input

impedance, then the input impedance of the at the terminal 401 will have the selected input impedance.

[0088] FIG. 4d shows a differential lowpass filter 204 that has a constant impedance according to embodiments of the present invention. The filter 204 includes a plurality *RLC* circuit units or poles 440a, 440b, 440c, etc., that are connected in series with each other between an input 401 and an output 402. Each pole 440 includes a first inductor 443, a second inductor 446, a capacitor 444, a resistor 445, along with other poles 440 that end in the termination resistor 206 and the PMOS relay device 273. The input signals come through input terminals 401a and 401b, wherein terminal 401a can serve as an input means for a positive differential component and input terminal 401b may serve as an input means for a negative differential potential. The output of the filter 204 is taken across output terminals 402a and 402b. The termination resistor 206 and the PMOS relay device are connected across the output terminals 402. As with the filters 204 shown in FIGS. 4b and 4c, each pole 440 maintains a constant impedance to an incoming signal, if the inductors 443, 446 and the capacitor 444 satisfy equations (5)-(7). When using equations 7 and 8, the calculated inductor values are divided by 2, and assigned to the inductors 443 and 446. For example, if the inductor value is calculated to be 7.0uH from equations 7 and 8, then the inductors 443 are set to 3.5uH and the inductors 446 are set to 3.5uH.

[0089] Filter 204 is illustrated to have 3 poles. However, any number of filter poles could be utilized. For example, filter 204 in FIG. 4e has four *RLC* poles 440 (a, b, c, d) connected in series between the input 401 and the output 402. Each pole 440 includes the first inductor 443, the second inductor 446, the capacitor 444, the resistor 445, along with other poles 440 that end in a termination resistor 206 and the PMOS relay device 273. Filter 204 of FIG. 4e is also a differential filter as is the one shown in FIG. 4d. An input differential signal comes in through terminals 401a and 401b and passes through each individual pole 440 (a,

b, c, d). The incoming signal after being filtered through each individual pole, is terminated in the termination resistor 206.

[0090] The values of each of the resistors 445 in both FIGS. 4d and 4e may differ as well as the values of inductors 443 and 446 and capacitors 444. However, the filters 204 of FIGS. 4d and 4e will have a constant input impedance as long as the relationship described by formula (7) is substantially maintained within each individual pole. Each pole in all of the embodiments of the present invention filter is independent of another pole, which makes the filter more advantageous over conventional filters. It is understood by one skilled in the art that the present invention is not limited to the embodiments shown in FIGS. 4a-4e, as other arrangements will be apparent to those skilled in the art based on the discussion given above. In embodiments of the invention, the filters described herein have at least two poles in order to avoid sensitivity of components in the filter.

[0091] The differential filters shown in FIGS. 4d and 4e have a better noise reduction parameters than single-ended filters, shown in FIG. 4b and 4c. The values of the elements comprising the poles 440 do not need to be the same, i.e., resistor in one pole does not need to be equal to the resistor in another pole. Nonetheless, as long as the relationship in equation (7) is preserved, each pole is independently preserving constant impedance through the entire chain of the poles.

[0092] The constant impedance of the present invention filter allows the filter to be connected to other circuitry at all times, without regard for unwanted signal reflections. For example, the present invention filter can be connected to the physical layer of an IP telephone system at all times. This is an advantage over the conventional filter, which utilizes off-chip relays to connect/disconnect the conventional filter to/from the physical layer, depending on the mode of operation. Since the present invention filter is connected at all times, this alleviates the connecting/disconnecting of the filter when the system changes its modes.

[0093] In one embodiment of the present invention, the values of the components of the filters 204 of FIGS. 4d and 4e may be as follows. The resistors 445 are of 100Ohm each. The capacitors 444 are of 700pF each. The inductors 443 and 446 are of 3.5u each. The mentioned vales will produce a constant input impedance of approximately 100 ohms at the input of the filters 204 of FIGS. 4d and 4e, according to equation (7). These values are provide for example purposes only, and are not meant to be limiting. Other filter component values will apparent to those skilled in the arts based on the discussion given herein.

[0094] Since, the filter poles are independent of one another, one can construct the filters according to a band of frequencies supplied to it. For example, if it is desired to have a filter accepting only 1MHz frequencies, then all poles would have a 1MHz passband response. If it is desired that the filter would have a gradual response to a range of 1MHz to 10MHz, each pole may have a different passband response according to the range.

[0095] Further description of constant impedance filters can be found in U.S. Application 09/986,752, filed November 9, 2001, which is incorporated by reference herein in its entirety.

Conclusion

[0096] Example embodiments of the methods, circuits, and components of the present invention have been described herein. As noted elsewhere, these example embodiments have been described for illustrative purposes only, and are not limiting. Other embodiments are possible and are covered by the invention. Such embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.